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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,926	03/30/2001	Giovanni Campardo	856063.689	7548

500 7590 03/27/2006

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EXAMINER	
LAMARRE, GUY J	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 03/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,926	CAMPARDO ET AL.	
	Examiner	Art Unit	
	Guy J. Lamarre	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 Nov. 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 2-27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 2-27 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is in response to Applicants' amendment of *14 Nov. 2005*.

1.1 **Claims 2-3, 6, 14-17, 19-20, 22** are amended, **Claims 23-27** are added, **Claims 2-27** remain pending in response to Applicants' election with traverse.

1.2 The prior art rejections of record are withdrawn in response to Applicants' amendment.

Response to Arguments

2. Applicants' arguments are moot in view of new ground of rejection via **NN74091034:** ***"Circuit Diagnosis and Design Analysis System;"*** IBM Tech. Discl. Bulletin, July 1987, US, VOL. 17 ISSUE: 4 Pgs: 1034 - 1035 ; September 1, 1974.

Claim Rejections - 35 USC ' 103

3.1 **Claims 2-27**_are rejected under 35 U.S.C. 103(a) as being unpatentable over as being unpatentable over **Applicants' Admitted prior art** (hereinafter **Admitted prior art**) and NN74091034: "*Circuit Diagnosis and Design Analysis System;*" (hereinafter **IBM Tech).**

As per Claims 2-27, Admitted prior art substantially discloses, at paras. 2-13, especially at para. 13, an equivalent memory device and testing method thereof comprising: internal data/testing/simulator circuitry and related internal/embedded conntroller circuitry to impose data/test vectors to device under test and sequencing operation (read/write/erase, program, simulate) circuitry, said memory device comprising logic and memory to be tested. {See **Admitted prior art,** paras. 2-13, in passim, wherein apparatus and method are described.}

Not specifically described in detail in **Admitted prior art** is the approach of whereby bypass/isolation circuitry is provided for external application of logic/memory test data and logic/memory simulation data via a control circuitry or instruction set to thereby bypass the embedded controller.

However IBM Tech, in an analogous art, discloses a "*Circuit Diagnosis and Design Analysis System,*" wherein such techniques are described. {See **IBM Tech,** Id., e.g., "*In normal operation, the isolation gates do not isolate semiconductor chips from each other and the circuit performs its intended function. However, in the case of uncertain or faulty operation, probe assembly 30 contacts the pads at the input and output of a selected semiconductor chip, such as chip 20. - The probe assembly connects the circuit pads to a set of input circuits 40 and a set of output circuits 50, under the control of an external simulator/tester 60. The isolation gate of circuits being bypassed are activated to operate in the bypass mode, and the substituted circuits are appropriately programmed to provide the functions which substitute for the circuits of chip 20. The programming may use several techniques such as plug boards, read-only memory or programmable controllers. As an alternate, a substitute chip or module 70 may be connected to provide altered design functions or a maintenance replacement for the functions of chip 20. This permits functional verification prior to the removal of the doubtful chip, module or circuit function. - An alternate isolation fan-out technique is illustrated in Fig. 2. This approach reduces the required quantity of chip pads and circuits. The isolation gate may be conditioned to enable the circuits in the assembly. The disable gate may be applied at individual chips to obtain the isolation of that chip so it may receive a normal substitute or simulated function, as illustrated by block diagram 80. The testing of the circuits of individual chips is accomplished by disabling the circuits using the isolation gate input. The enable gate of the individual chip is actuated to permit the normal testing of the selected chip. - Another alternate fan-out technique is illustrated in Fig. 3. This approach further reduces the required quantity of chip pads and circuits. The testing of an individual chip is accomplished by switching the isolation gate driver 100 to a state which isolates all of the chip output circuits. Then the circuits of the individual chip to be tested 120 are contacted, and the isolation gate input is switched to the state which activates chip 120 for normal testing. - The bypassing of the function of an individual chip is accomplished by switching the isolation gate driver 100, to a state which enables all of the chip output circuits. Then the circuits of the individual chip to be bypassed e.g., 130, are contacted and the isolation gate input signal is conditioned to the state which deactivates the normal functions of chip 130. This*

permits signals to be monitored at the signal inputs of the chip and signals to be injected at the chip output circuits, as described above.... "}

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure in the **Admitted prior art** by including therein bypass/isolation circuitry for external application of test data and simulation data via a control circuitry or instruction set as taught by **IBM Tech,** because such modification would provide the procedure disclosed in **Admitted prior art** with a technique whereby it is possible for "*signals to be monitored at the signal inputs of the chip and signals to be injected at the chip output circuits ....*" {See **IBM Tech,** last sentence.}

Conclusion

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (703) 872-9306 for all formal communications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (571) 272-3826. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached at (571) 272-3819.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Guy J. Lamarre, P.E
Primary Examiner
3/6/2006